SRI BHAGAWAN MAHAVEER JAIN COLLEGE Vishweshwarapuram, Bangalore. **Mock Paper-2 (2017-18)**	**Course:**	II PUC
	Subject:	**Electronics**
	Max. Marks:	70
	Duration:	3hrs

Note: 1) Question paper has **four** parts **A, B, C** and **D**.

2) Part - **A** is **compulsory.**

3) Part - **D** has **two** parts. Part- **I** is from **problems.**

Part- **II** is of **essay type** questions.

4) Circuit diagrams/timing diagrams/truth tables should be drawn **wherever** necessary.

5) Problems without **necessary** formula/formulae carry **no mark**.

PART- A

I. Answer **all** questions: **(10x1=10)**

1. What is the purpose of R_c in voltage divider bias circuit for a BJT?
2. Define common mode gain.
3. If the maximum frequency of baseband signal is 5 KHz what is the BW of AM?
4. What is the frequency spectrum allotted for commercial FM?
5. Draw the circuit symbol of IGBT.
6. Write XS3 code for $11_{(10)}$.
7. Name any one application of Gray code.
8. What is PC in 8015 microcontroller?
9. Name any one backslash constant in C programming.
10. What is 'domain' in internet address?

PART- B

II. Answer any **FIVE** questions: **(5x2=10)**

11. Define amplification factor for JFET. What is I_{DSS}?
12. List any two limitations of direct coupling in amplifiers.
13. Define loop gain. What kind of feedback is used for oscillators?
14. State Barkhausen criterion for sustained oscillations.
15. Define percentage modulation for FM. What is the maximum allowed Δf for FM broadcast?
16. Draw the forward characteristics of SCR.
17. Write the C syntax for **if else**.
18. Write any two difference between WiFi and Bluetooth.

PART- C

III. Answer any **FIVE** questions: **(5x3=15)**

19. What is DC load line? Write the expression for $I_{c(sat)}$ and $V_{CE(cutoff)}$ for a CE amplifier with voltage divider bias circuit.
20. Derive an expression for output impedance of voltage series negative feedback amplifier.

21. Write a note on space waves.
22. Explain two transistor model of SCR.
23. Explain the working of full wave controlled rectifier using SCR.
24. Write the pin diagram of IC 7400 and construct AND and XOR gates using NAND gates.
25. List the meaning of any three bits in PSW with their bit positions.
26. Explain call hand-off in mobile communication system.

PART- D

VI. Answer any **THREE** questions: **(3x5=15)**

27. A three stage amplifier has a first stage voltage gain of 10, second stage gain of 50 and third stage gain of 400. If the input voltage for the first stage is 10μV, determine the output voltage at each stage. Also find the total voltage gain.
28. Design an OpAmp scaling amplifier whose output is to be $V_o = 3.3V_1-2V_2+0.5V_3$. Asume the $R_F = 15K\Omega$.
29. A Hartley oscillator generates a frequency of 108 MHz If the value of one of the inductor is 12μH and C = 12μF, determine the value of other inductor and the gain required for sustained oscillations.
30. A modulating signal $10\sin(2\pi 10^3 t)$ is used to amplitude modulate a carrier signal $20\sin(2\pi 10^6 t)$. Find modulation index, percentage modulation, frequency of the sidebands with their amplitudes and bandwidth of the modulated signal.
31. Simplify Y(ABCD)=$\sum m(3,4,5,7,9,13,14) + \sum d(15)$ using K-map and draw the logic circuit for the simplified expression using NAND gates only.

PART- D

V. Answer any **FOUR** questions: **(4x5=20)**

32. With a neat circuit diagram explain the working of common source FET amplifier.
33. Derive an expression for the output voltage of op-amp anti-logarithmic amplifier.
34. Draw the block diagram of FM SHD receiver and explain the working of each block.
35. Explain the working of master-slave JK flip flop with truth table and timing diagram.
36. What is addressing mode? List the types of addressing modes in 8051 with an example.
37. Write a C program to accept three integers and to determine smallest among them.

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